Docket No.: 61282-011

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Kenji SHIMAZAKI, et al. :

Serial No.: : Group Art Unit:

Filed: March 08, 2001 : Examiner:

For: ELECTROMAGNETIC INTERFERENCE ANALYSIS METHOD AND APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, DC 20231

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Respectfully submitted,

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SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
61282-011	
APPLICANT: Kenji SHIMAZAKI, et al.	
FILING DATE: March 08, 2001	GROUP

J1044 U.S. PTO 09/801200

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,412,589	5/2/95	Williams et al.			
	5,675,832	10/7/97	Ikami et al.			
	5,699,263	12/16/97	Nakao			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	"*di/dt* Noise in CMOS Integrated Circuits", by Patrik Larsson, Analog Integrated Circuits and Signal Processing, Vol. 14 (1997), pp. 113-129.
	"EMI-Noise Analysis Under ASIC Design Environment", by Sachio Hayashi et al., International Symposium on Physical Design (1999), pp. 16-21.
	"Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design", by Howard Chen et al., DAC97, pp. 1-6.
	"Design Methodologies for Noise in Digital Integrated Circuits", by Kenneth Shepard, DAC98 (June 1998).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.